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SPECIFICATION

TITLE OF THE INVENTION

INTERLEAVING METHOD AND APPARATUS, DE-INTERLEAVING METHOD AND APPARATUS, AND INTERLEAVING/DE-INTERLEAVING SYSTEM AND APPARATUS

BACKGROUND OF THE INVENTION

(1) Field of the Invention

The present invention relates to an interleaving method and a de-interleaving method, an interleaving apparatus and a de-interleaving apparatus, an interleaving/de-interleaving system, and an interleaving/de-interleaving apparatus, which can suitably rearrange a data array.

(2) Description of Related Art

In radio communications, there is a case where data transmitted from a transmitter to a receiver is affected by fading during transmission so that the data is changed to erroneous data differing from received contents.

As a technique dealing with fading, there are interleaving and de-interleaving. Interleaving is a technique of rearranging an order of data to be transmitted, and outputting the data when the data is transmitted from a transmitter, for example. On the other hand, de-interleaving is a technique of

rearranging an order of the interleaved data transmitted from the transmitter back to an order before interleaved.

Interleaving is classified into block-interleaving and random-interleaving.

Block interleaving is to regularly rearrange an array of data.

For example, data before block-interleaved are "D0, D1, D2, D3, … and D383". Incidentally, the data will be described as "0, 1, 2, 3, … and 383", hereinafter.

These 384 (0-383) of data are assumed to be, as shown in FIG. 22, arranged in a matrix of 24 rows by 16 columns in a storing unit. When written, the data is rearranged in order in the direction of rows, and read out from each column (A′-P′) in order.

The data read out is rearranged into "000", "016", "032", "048", "064", "080", "096", "112", "128", "144", "160", "176", … "351", "367", and "383". In a sequence of interleaved data, data numbers having been spaced at mostly 15 of data are arranged such as "000", "016", "031" and so on.

When reading of the last data "368" in the column A′ is completed in reading the data, the leading data "001" in column B′ is next read out. At the ending/beginning of other column, the data is read out in the similar manner. When the last data "383" is

read out, the leading data in column A′ is next read out.

On the other hand, when the receiver receives block-interleaved data, the receiver rearranges the data in the order of the data before interleaved by performing the reverse processing.

The block-interleaved data is affected by fading during transmission while transmitted from the transmitter to the receiver, changed into contents different from the transmitted contents, and received with burst errors by the receiver. Assuming that burst errors generate in the data in column B′ (001, 017, 033, 049, 065, 081, 097, 113, 129, 145, 161, 177, 193, 209, 225, 241, 257, 273, 289, 305, 321, 337, 353 and 369) shown in FIG. 22, for example.

The receiver de-interleaves the received data to rearrange the data in the order before interleaved in the transmitter (000, 001, 002, 003, 004, … 381, 382 and 383).

The erroneous data continuously generated in the transmitted data is thereby regularly distributed. Namely, the erroneous data is spaced at every 15 data numbers so as to be distributed and arranged in the data (000-383).

The erroneous data is corrected by an error correcting function in consideration of a relation with the preceding/following data.

Accordingly, block interleaving/block de-interleaving facilitate correction of continuous errors by regularly distributing the errors, as above.

When burst errors generate in the leading data "001" in column B' to the data "130" in column C', for example, the erroneous data distributed in the de-interleaved data "0-383" might be continuously placed as "001" and "002". In such case, it possibly occurs that the errors cannot be corrected by the error correcting function.

On the other hand, random interleaving is to randomly rearrange an array of data.

FIG. 23 is a diagram illustrating random interleaving. As shown in FIG. 23, random interleaving is to rearrange the data by writing the data in the order of described numbers in a storing unit and reading the data in alphabetical order.

In the case where the data is randomly written in the storing unit in random interleaving, the data "0-383" is randomly written in a matrix of 24 rows by 16 columns in the storing unit, as shown in FIG. 24, for example.

If the data is read out in the order arranged in the row when read out from the storing unit, the data read out is rearranged in the order of "000", "255", "127", "063", "031", "015", "263", "240", "376", "251", "125", …, "123", "061", "030" and "271".

The random-interleaved data are rearranged, not following the rule that the block-interleaved data is spaced at every 15 data numbers, when compared with the block-interleaved data.

When reading of the last data "232" in the first row is completed in reading the data, the leading data "116" in the second row is then read out. The reading of the ending/beginning of the data in other row is performed in the similar manner. When the last data "271" is read out, the leading first row is next read out.

On the other hand, when the receiver receives the random-interleaved data, the data random-interleaved is rearranged in the order of the data before random-interleaved in the reverse processing.

The random-interleaved data is affected by fading during transmission when transmitted from the transmitter to the receiver so as to be changed to contents different from the transmitted contents, and received with burst errors by the receiver. Assuming that burst errors generate in the data in the second row (116, 314, 206, 103, 307, 153, 076, 038, 019, 009, 026, 130, 065, 288, 144 and 328) shown in FIG. 24, for example.

The receiver de-interleaves the received data to rearrange the data in the order before interleaved in the transmitter (000, 001, 002, 003, 004, …, 381,

382 and 383).

The erroneous data (116, 314, 206, 103, 307, 153, 076, 038, 019, 009, 260, 130, 065, 288, 144 and 328) having continuously generated in the transmitted data is irregularly distributed in the data (000-383).

The erroneous data is corrected by the error correcting function in consideration with a relation with the preceding/following data.

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Next, assuming that burst errors generate in the data (198, 099, 305, 152, 332, 166, 083, 041, 276, 197, 354, 177, 088, 300, 150 and 331) in the 14th row shown in FIG. 14.

The erroneous data is distributed in the data (000-383), but each erroneous data is placed in the neighboring positions to each other when rearranged into the state before random-interleaved.

Namely, "083" and "088", "150" and "152", "197" and "198", "300" and "305", and "331" and "332" in the erroneous data are distributed in totaling 384 (000-383) of data, but the erroneous data is placed in the neighboring positions to each other, which cannot be possibly corrected by the error correcting function.

In such case, errors having generated in bursts are randomly distributed in random interleaving/random de-interleaving. However, positions of the distributed errors are locally close

to each other, which leads to deviation of the distribution.

Next, assuming that 65536 (256 x 256) of data are arranged in a matrix of 256 rows by 256 columns in the storing unit.

When

$i' = 129(i + j) \bmod 256$ … (1)

$j' = [P(\xi) \cdot (i + 1)] - 1 \bmod 256$ … (2),

the data is written in the order of the i-th row and the j-th column, and read out in the order of the i1-th row and the j1-th column.

In the above formulae (1) and (2), $\xi = (i + j)$ mode 8, $P(0) = 17$, $P(1) = 37$, $P(2) = 19$, $P(3) = 29$, $P(4) = 41$, $P(5) = 23$, $P(6) = 13$ and $P(7) = 7$ (i, j, i', j' = 0, 1-8).

The data is written in the storing unit in the order of the i-th row and the j-th column (the 1st column and the 1st row, the 1st row and the 2nd column, …, the 1st row and the 256th column, the 2nd row and the 1st column, … and the 256th row and the 256th column), and read out in the order of the i'-th row and the j'-th column from the storing unit.

(X mod y) represents a remainder generated when x is divided by y.

However, fabrication of an interleaving apparatus which reads according to the above formulae (1) and (2) is not easy since a manner of random

generation is complicated.

Fabrication of a de-interleaving apparatus which de-interleaves the data interleaved in the above manner is also not easy.

SUMMARY OF THE INVENTION

In the light of the above problems, an object of the present invention is to prevent biased distribution of data by using relatively easy interleaving in a simple structure.

The present invention therefore provides an interleaving method comprising the steps of arranging data to be transmitted in a matrix, and randomly rearranging at least either columns or rows of the data and outputting the rearranged data in time series.

According to the interleaving method of this invention, data to be transmitted is rearranged by arranging the data to be transmitted in a matrix and randomly rearranging at least either columns or rows thereof, and outputted in time series, by using relatively easy interleaving even if burst errors are generated in the data to be transmitted due to an effect of fading during transmission, thereby preventing biased distribution of the data which leads to degradation of the transmission quality.

The present invention further provides a de-interleaving method comprising the steps of

arranging received data having been interleaved in a matrix, and randomly rearranging at least either columns or rows of the data, and outputting the data in time series, thereby outputting the received data in the order before the received data was interleaved.

According to the de-interleaving method of this invention, received data having been interleaved is arranged in a matrix, at least either columns or rows thereof are randomly rearranged, and the data is outputted in time series, by using relatively easy de-interleaving, thereby preventing biased distribution of error data which leads to degradation of the transmission quality.

The present invention still further provides an interleaving apparatus for interleaving data to be transmitted comprising a first storing unit for storing data to be transmitted, and a first control unit for controlling the first storing unit so that the data to be transmitted is outputted from the first storing unit with the data to be transmitted arranged in a matrix and at least either columns or rows of the data to be transmitted randomly rearranged.

According to the interleaving apparatus of this invention, the first control unit controls the first storing unit to output the data to be transmitted from the first storing unit with the data to be transmitted arranged in a matrix and at least either

columns or rows thereof randomly rearranged, by using relatively easy interleaving in a simple structure, thereby preventing biased distribution of error data which leads to degradation of the transmission quality.

The present invention still further provides a de-interleaving apparatus for de-interleaving received data comprising a second storing unit for storing the received data, and a second control unit for controlling the second storing unit so that the received data is outputted from the second storing unit in a state before the receive data was interleaved by arranging the received data in a matrix and randomly rearranging at least either columns or rows of the received data.

According to the de-interleaving apparatus of this invention, the second control unit controls the second storing unit to output the received data from the second storing unit in a state before the received data was interleaved by arranging the received data in a matrix and randomly rearranging at least either columns or rows thereof, by using relatively easy de-interleaving in a simple structure, thereby preventing biased distribution of error data which leads to degradation of the transmission quality.

The present invention still further provides an interleaving/de-interleaving system comprising an

interleaving apparatus for interleaving data to be transmitted and a de-interleaving apparatus for receiving the transmitted data interleaved by the interleaving apparatus to de-interleave the transmitted data, wherein the interleaving apparatus outputs the data to be transmitted with the data to be transmitted arranged in a matrix and at least either columns or rows of the data to be transmitted randomly rearranged, and the de-interleaving apparatus outputs received data in a state before the transmitted data was interleaved by arranging the received data in a matrix and randomly rearranging at least either columns or rows of the received data.

According to the interleaving/de-interleaving system of this invention, the interleaving apparatus outputs the data to be transmitted with the data to be transmitted arranged in a matrix and at least either columns or rows thereof randomly rearranged, while the de-interleaving apparatus outputs received data in a state before interleaved by arranging the received data in a matrix and randomly rearranging at least either columns or rows thereof. It is thereby possible to prevent biased distribution of data relatively easily in a simple structure even if burst errors generate in interleaved data, which leads to prevention against degradation of the transmission quality.

The present invention still further provides an interleaving/de-interleaving apparatus for transmitting/receiving interleaved data to/from an opposite interleaving/de-interleaving apparatus comprising an interleaving apparatus for outputted data to be transmitted to the opposite interleaving/de-interleaving apparatus with the data to be transmitted arranged in a matrix, and at least either columns or rows of the data to be transmitted randomly rearranged, and a de-interleaving apparatus for outputting received data interleaved in the opposite interleaving/de-interleaving apparatus in a state before the received data was interleaved by arranging the received data in a matrix, and randomly rearranging at least either columns or rows of the received data.

According to the interleaving/de-interleaving apparatus of this invention, the interleaving apparatus and the de-interleaving apparatus randomly rearrange data to be transmitted and randomly rearrange received data, thereby preventing degradation of the transmission quality of the transmitted data and received data.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a block diagram showing an aspect of an interleaving apparatus according to this

invention;

FIG. 2 is a block diagram showing an aspect of a de-interleaving apparatus according to this invention;

FIG. 3 is a block diagram showing an aspect of an interleaving/de-interleaving system according to this invention;

FIG. 4 is a block diagram showing an aspect of an interleaving/de-interleaving apparatus according to this invention;

FIG. 5 is a block diagram showing a structure of an MS according to a first embodiment of this invention;

FIGS. 6 through 8 are diagrams for illustrating interleaving performed in an interleaving unit according to the first embodiment of this invention;

FIG. 9 is a diagram showing data interleaved by the interleaving unit according to the first embodiment of this invention;

FIG. 10 is a block diagram showing an interleaving apparatus according to the first embodiment of this invention;

FIG. 11 is a block diagram showing a detailed structure of a first RAM read processing unit according to the first embodiment of this invention;

FIGS. 12(a) through 12 (d) are time charts for

illustrating a schematic operation of a shift register in a one row generating circuit according to the first embodiment of this invention;

FIG. 13 is a block diagram showing a de-interleaving apparatus according to the first embodiment of this invention;

FIG. 14 is a block diagram showing a structure of a de-interleaving unit according to a first modification of the first embodiment of this invention;

FIG. 15 is a diagram showing values outputted from an A column generating circuit, a one row generating circuit and an adder according to the first modification of the first embodiment of this invention;

FIG. 16 is a block diagram showing a structure of an interleaving unit according to the first modification of the first embodiment of this invention;

FIG. 17 is a block diagram showing a de-interleaving unit according to a second embodiment of this invention;

FIG. 18 is a block diagram showing an interleaving apparatus according to the second embodiment of this invention;

FIG. 19 is a block diagram showing an error correction encoding unit having an interleaving

function according to another embodiment of this invention;

FIG. 20 is a block diagram showing an error correction decoding unit having an interleaving function and a de-interleaving function according to another embodiment of this invention;

FIG. 21 is a block diagram showing an interleaving unit according to still another embodiment of this invention;

FIG. 22 is a diagram for illustrating block interleaving;

FIGS. 23 and 24 are diagrams for illustrating random interleaving; and

FIG. 25 through 32 are diagrams for illustrating interleaving (24[4[2×2]x6[3×2]]x 16[4[2×2]×4[2×2]]).

DESCRIPTION OF THE PREFERRED EMBODIMENTS

(a) Description of Aspects of the Invention

Hereinafter, description will be made of aspects of the present invention with reference to the drawings.

FIG. 1 is a block diagram showing an aspect of an interleaving apparatus according to this invention. In FIG. 1, an interleaving apparatus 1 interleaves data to be transmitted, which has a first storing unit 2 for storing the data to be transmitted,

and a first control unit 3 for controlling the first storing unit 2 to output the data to be transmitted from the first storing unit 2 with the data to be transmitted arranged in a matrix and at least either columns or rows thereof randomly rearranged. Incidentally, data to be transmitted (D000-D383) shown in FIG. 1 is merely an example.

Accordingly, in the interleaving apparatus 1, the first control unit 3 controls the first storing unit 2 to output the data to be transmitted from the first storing unit 2 with the data to be transmitted arranged in a matrix and at least either columns or rows thereof randomly rearranged, by using relatively easy interleaving in a simple structure, thereby preventing biased distribution of error data which leads to degradation of the transmission quality.

FIG. 2 is a block diagram showing an aspect of a de-interleaving apparatus according to this invention. In FIG. 2, a de-interleaving apparatus 4 de-interleaves received data. The de-interleaving apparatus 4 has a second storing unit 5 for storing the received data, and a second control unit 6 for controlling the second storing unit 5 to output the received data in a state before the received data was interleaved from the second storing unit 5 by arranging the received data in a matrix, and randomly rearranging at least either columns or rows thereof.

Incidentally, received data (D000-D383) shown in FIG. 2 is merely an example.

Accordingly, in the de-interleaving apparatus 4, the second control unit 6 controls the second storing unit 5 to output the received data in a state before interleaved from the second storing unit 5 by arranging the received data in a matrix and randomly rearranging at least either columns or rows of thereof, by using relatively easy de-interleaving in a simple structure, thereby preventing biased distribution of error data which leads to degradation of the transmission quality.

FIG. 3 is a block diagram showing an aspect of an interleaving/de-interleaving system according to this invention. In FIG. 3, an interleaving/de-interleaving system 7 has an interleaving apparatus 1 for interleaving data to be transmitted, and a de-interleaving apparatus 4 for receiving the transmitted data interleaved in the interleaving apparatus 1 to de-interleave the data, wherein the interleaving apparatus 1 outputs the data to be transmitted with the data to be transmitted arranged in a matrix, and at least either columns or rows thereof randomly rearranged, and the de-interleaving apparatus 4 outputs received data in a state before the transmitted data was interleaved by arranging the received data in a matrix, and randomly rearranging

at least either columns or rows thereof.

Accordingly, in the interleaving/de-interleaving system 7, the interleaving apparatus 1 outputs the data to be transmitted with the data to be transmitted arranged in a matrix, and at least either columns or rows thereof randomly rearranged, whereas the de-interleaving apparatus 4 outputs the received data in a state before the transmitted data was interleaved by arranging the received data in a matrix, and randomly rearranging at least either columns or rows thereof, thereby preventing biased distribution of data which leads to degradation of the transmission quality, relatively readily, in a simple structure even when burst errors generate in the interleaved data.

FIG. 4 is a block diagram showing an aspect of an interleaving/de-interleaving apparatus according to this invention. In FIG. 4, an interleaving/de-interleaving apparatus 8A transmits/receives interleaved data to/from an opposite interleaving/de-interleaving apparatus 8B. The interleaving/de-interleaving apparatus 8A has an interleaving apparatus 1 for outputting data to be transmitted to the opposite interleaving/de-interleaving apparatus 8B with the data to be transmitted arranged in a matrix, and at least either columns or rows thereof randomly rearranged, and a

de-interleaving apparatus 4 for outputting received data having been interleaved in the opposite interleaving/de-interleaving apparatus 8B in a state before the received data was interleaved by arranging the received data in a matrix, and randomly rearranging at least either columns or rows thereof.

Accordingly, in the interleaving/de-interleaving apparatus 8A or 8B, the interleaving apparatus 1 and the de-interleaving apparatus 4 randomly rearrange data to be transmitted, and randomly rearrange an array of received data, thereby preventing degradation of the transmission quality of the data to be transmitted and the received data.

(b) Description of Embodiments of the Invention

Hereinafter, embodiments of this invention will be described with reference to the drawings.

(b1) Description of a First Embodiment

A first embodiment will be described by way of an example in which a mobile station and a base station carry out CDMA (Code Division Multiple Access) connection using a spread spectrum technique in a portable telephone system.

The following description will be made in the case where signals are transmitted/received between each mobile station (MS) and the base station (BS).

FIG. 5 is a block diagram showing a structure of an MS according to the first embodiment. As shown

in FIG. 5, the MS 50 comprises a receiver 50-a, a de-spreader 50-b, a data extracting unit 50-c, a de-interleaving unit 50-d, an error correction decoding unit 50-e, an error detecting unit 50-f, a CPU 50-g, an error detection encoding unit 50-h, an error correction encoding unit 50-i, an interleaving unit 50-j, a signal assembling unit 50-k, a spreader 50-l, a transmitter 50-m, a duplexer 50-n and an antenna 50-p.

The receiver 50-a modifies a signal received via the antenna 50-p and the duplexer 50-n into a signal easily processable by the de-spreader 50-l.

For example, the receiver 50-a not only down-converts a signal (radio frequency received signal: RF signal) received via the antenna 50-p and the duplexer 50-n into an intermediate frequency signal (IF signal) to separate the signal into I channel components and Q channel components, but also converts each of the components (I channel components and Q channel components) from analog to digital to generate a digital signal.

Next, the de-spreader 50-b separates a desired signal from a digital signal sent from the receiver 50-a using a de-spreading code. The data extracting unit 50-c extracts data from the signal separated by the de-spreader 50-b.

The error correction decoding unit 50-e

decodes data de-interleaved by the de-interleaving unit 50-d, and corrects an error included in the data using an error correcting code. For example, an error is corrected using a parity check bit added when data (main signal) is transmitted, and the parity check bit is deleted in decoding and correcting.

The error detecting unit 50-f detects an error detecting bit added when the data (main signal) is transmitted on the basis of a bit structure of the error detecting bit previously set. Information or data about an error or the like detected by the error detecting unit 50-f is notified the CPU 50-f.

The error detection encoding unit 50-h encodes the error detecting bit to be used to detect an error and adds the error detecting bit to data sent from the CPU 50-g. The error correction encoding unit 50-i adds the error correcting code, which is to be used for error correction, to the data sent from the error detection encoding unit 50-h.

The signal assembling unit 50-k assembles interleaved data to form a signal format suited for transmission. The spreader 50-l converts a signal sent from the signal assembling unit 50-k into a spread signal using a predetermined spreading code.

The transmitter 50-m modifies a signal sent from the spreader 50-l into a signal to be transmitted.

For example, the transmitter 50-m converts each component (I channel or Q channel) of a digital signal sent from the spreader 50-1 into an analog signal in digital/analog conversion. The transmitter 50-m up-converts an intermediate frequency signal (IF signal) into a radio frequency signal (RF signal) after orthogonal-modulating the signal into an orthogonal-modulated signal.

The radio frequency signal is transmitted to the outside via the duplexer 50-n and the antenna 50-p.

The interleaving unit (interleaving apparatus) 50-j interleaves data to be transmitted.

In concrete, the interleaving unit 50-j arranges data to be transmitted in a matrix, randomly rearranges rows and columns of the data, and outputs the rearranged data in time series.

Assuming that a series of data to be transmitted consists of 384 (000-383) of data.

The data (000-383) is, as shown in FIG. 6, arranged in a matrix (16 columns by 24 rows), after that, columns of the data are rearranged, as shown in FIG. 7. As shown in FIG. 6, the columns (A to P) are arranged in alphabetical order, but the data is rearranged in the order of A, P, J, … and so on by rearranging the columns of the data, as shown in FIG. 7.

After that, the rows of the data (000-383) are rearranged, as shown in FIG. 8. As shown in FIG. 7, the rows (1-24) are arranged in the order numbered, but the rows are rearranged in the order of 1, 16, 19, 10, 17, … and so on by the rearranging the rows, as shown in FIG. 8.

The data arranged in a matrix as shown in FIG. 8 is read out in order column by column, beginning with "000" in column A, whereby the order in which the data has been arranged is randomly rearranged. Namely, the read data is irregularly rearranged, as shown in FIG. 9.

FIG. 10 is a block diagram showing the interleaving apparatus 50-j according to the first embodiment of this invention. As shown in FIG. 10, the interleaving apparatus 50-j comprises an interleaving RAM (Random Access Memory) 51 and a control processing unit 52.

The interleaving RAM (first storing unit) (hereinafter referred as "first RAM 51") stores data to be transmitted.

The control processing unit (first control unit) 52 (hereinafter referred as "first control processing unit") controls the first RAM 51 so that the data to be transmitted is transmitted from the first RAM 51 with the data to be transmitted arranged in a matrix and rows or columns thereof randomly

rearranged.

To this end, the first control processing unit 52 comprises a write processing unit 60 (hereinafter referred as "first write processing unit") and a read processing unit 70 (hereinafter referred as "first read processing unit 70).

The first write processing unit 60 performs a control to write data in the first RAM 51, which outputs an address and an enable signal (not shown). The first writing processing unit 60 writes signals sent from the error correction encoding unit 50-i in order of addresses.

To this end, the first write processing unit 60 comprises a counter 61, as shown in FIG. 10. The counter 61 generates count values from "0" to "383". The counter 61 counts up the value in ascending order, and again counts from "0" when the count value reaches the maximum value.

Each of the count values (0-383) is used as an address for input data. The first data "000", for example, is stored in the 0th address with a count value "0" outputted from the counter 61 as an address. The 107th data is stored in the 106th address with a count value "106" as an address.

The read processing unit (first read processing unit) 70 generates an address used to read the data to be transmitted from the first RAM 51 with

the data to be transmitted stored in the first RAM 51 arranged in a matrix and columns and rows thereof randomly rearranged, so as to read the data.

The first read processing unit 70 reads the data (refer to FIG. 6) having been arranged in a matrix and held in the first RAM 51 from the first RAM 51 in a data array shown in FIG. 9.

To this end, the first read processing unit 70 comprises an A column generating circuit 71, a one row generating circuit 72 and an adder 73.

The A column generating circuit (column number generating unit) 71 randomly generates a column number, which generates any one of 24 numbers (a multiplex of 16 or 000 among 000-383) in column A shown in FIG. 8. The A column generating circuit 71 generates 24 numbers in column A within one cycle , then is reset when completing generation of 24 numbers and shifting to the next cycle, and again outputs 24 numbers in column A. Additionally, the A column generating circuit 71 outputs a carry pulse to the one row generating unit 72 when the cycle is changed.

The one row generating unit (row number generating unit) 72 generates a row number, which generates any one of 16 numbers (000-015) in one row shown in FIG. 8. The one row generating unit 72 randomly changes row numbers to be outputted each

time all 24 column numbers in column A are outputted (in each cycle of the A column generating circuit 71). When the one row generating circuit 72 completes generation of 16 numbers (000-015), the one row generating circuit 72 is reset, thereby again outputting 16 numbers in one row.

The adder 73 outputs a value obtained by adding numbers outputted from the A column generating circuit 71 and the one row generating circuit 72 as a read address for the first RAM 51.

Table 1 below shows an example of data outputted from the A column generating circuit 71, the one row generating circuit 72 and the adder 73.

[table 1]

Example of output data

	t1	t2	t3	…	t22	t23	t24	t25	t26	t27	…	t46	t47
Output of A column generating circuit	000	240	288	…	112	304	368	000	240	288	…	112	304
Output of one row generating circuit	000	000	000	…	000	000	000	015	015	015	…	015	015
Output of adder	000	240	288	…	112	304	368	015	255	303	…	127	319

As shown in Table 1 above, during timings t1 to t24, the A column generating circuit 71 outputs a different column number at each timing, whereas the one row generating circuit 72 outputs the same row number. At a timing t25 when 24 numbers having been outputted from the A column generating circuit 72

have taken a round, the one row generating circuit 72 outputs the next number. While numbers sent from the A column generating circuit 71 are taking a round (one cycle), the same number is outputted from the one row generating circuit 72. Only after numbers for 24 cycles are outputted from the A column generating circuit 71, the one row generating circuit 72 completes outputting of numbers (16 numbers from 000 to 015) for one cycle.

Although numbers or the like outputted from the circuits 71 and 72, and the adder 73 after a timing t47 in Table 1 above, the A column generating circuit 71 outputs 24 numbers in a cycle, whereas the one row generating circuit 72 outputs the same number in the same cycle, and outputs a different number each time the cycle is changed.

When attention is given to a timing t26 in Table 1 above, a value (read address) outputted from the adder 73 is a sum of "240" outputted from the A column generating circuit 71 and "015" outputted from the one row generating circuit 72.

FIG. 11 is a diagram showing a detailed structure of the first read processing unit 70 according to the first embodiment of this invention. The first read processing unit 70 shown in FIG. 11 comprises the A column generating circuit 71, the one row generating circuit 72, the adder 73 and an AND

circuit 74.

The A column generating circuit 71 comprises, as shown in FIG. 11, an EX-OR (exclusive OR) circuit (hereinafter referred merely as "EX-OR") 75-a, a shift register 75-b, a setting control unit 75-c, a first selecting circuit 71-a, a second selecting circuit 71-b, a third selecting circuit 71-c and an AND circuit 71-d. The A column generating circuit 71 generates 24 numbers (refer to FIG. 8) in column A using data of 9 bits.

The shift register 75-b holds data of 9 bits, which comprises flip-flops (hereinafter referred as "FF") 75-b1 through 75-b9.

The FFs 75-b1 through 75-b9 each holds a bit of "1 (High)" when activated under a control of the setting control unit 75-c performing a control when the apparatus is activated.

Data held in the shift register 75-b is successively shifted according to a clock (CLK). Bits outputted from the FF 75-b9 and the FF 75-b6 undergo an exclusive-OR operation in the EX-OR 75-a, then a resulting bit is held as a lower bit in the FF 75-b1.

Table 2 below shows an example of transition of a bit structure held in the shift register 75-b.

[Table 2]

Example of transition of a bit structure

Lower Order Higher Order				
111111111	001111111	000011111	000000111	110000001
011111111	000111111	000001111	100000011	

The first to third selecting circuits 71-a through 71-c and the AND circuit 71-d monitor data of 9 bits outputted from the A column generating circuit 71.

The first selecting circuit 71-a determines whether or not a numerical value represented by data (binary number) of 9 bits corresponds to a multiple of 16 and 0 as decimal numbers. In concrete, the first selecting circuit 71-a determines whether or not lower 4 bits among 9 bits are all "0". When the lower 4 bits are all "0", the first selecting circuit 71-a outputs a pulse (described as "pulse when YES" in FIG. 11).

The second selecting circuit 71-b determines whether or not a numerical value represented by data (binary number) of 9 bits is any numerical value among 0 to 368 as decimal numbers.

The third selecting circuit 71-b determines whether or not the 9 bits are all "1 (High)". When the 9 bits are all "1", the third selecting circuit 71-b outputs a pulse (carry pulse) (described as "pulse when YES" in FIG. 11).

Next, the one row generating circuit 72 shown in FIG. 11 comprises, similarly to the A column generating circuit 71, an EX-OR 75-a, a shift register 75-b and a setting control unit 75-c. In addition, the one row generating circuit 72 comprises a fourth selecting circuit 72-a and a switch (SW) 72-b.

The switch 72-b performs a control to send a clock (CLK) signal to the shift register 75-b according to a pulse outputted from the third selecting circuit 71-c or the fourth selecting circuit 72-a. When receiving a pulse signal from the third selecting circuit 71-c, the switch 72-b sends a clock signal to the shift register 75-b (ON control). When receiving a pulse signal from the fourth selecting circuit 72-a, the switch 72-b prevents a clock signal from passing therethrough (OFF control).

The fourth selecting circuit 72-a determines whether or not a numerical value represented by data (binary number) of 9 bits corresponds to any one of 0 to 15 as decimal numbers. In concrete, the fourth selecting circuit 72-a determines whether or not bits higher than lower 5 bits among the 9 bits include "1". When the bits higher than the lower 5 bits do not include "1", the fourth selecting circuit 72-a outputs a pulse signal (described as "pulse when YES"

in FIG. 11).

FIGS. 12(a) through 12(d) are time charts for illustrating a schematic operation of the shift register 75-b in the one row generating circuit 72. FIG. 12(a) shows a timing at which a pulse signal is outputted from the third selecting circuit 71-c. FIG. 12(b) shows a timing at which a pulse signal is outputted from the fourth selecting circuit 72-a. FIG. 12(c) shows a timing at which a clock signal is outputted from the switch 72-b. FIG. 12(d) is a time chart showing transition timings for data held in the shift register 75-b.

As shown in FIG. 12(a), when a pulse signal is outputted from the third selecting circuit 71-c at a timing T1, the switch 72-b sends a clock signal to the shift register 75-b in ON control [refer to FIG. 12(c)]. Each time the shift register 75-b receives a clock via the switch 72-b, the shift register 75-b shifts the data to change the data structure of 9 bits held therein [described as "points of change of data" in FIG. 12(d)].

On the other hand, as shown in FIG. 12(b), when a pulse signal is outputted from the fourth selecting circuit 72-a at a timing T2, the switch 72-b changes its state from where the switch 72-b sends a clock signal before the timing T2 to where the switch 72-b does not send a clock signal to the shift register

75-b [refer to FIG. 12(c)], so that the shift register 75-b does not shift the data but keeps the preceding state (does not change the data).

After that, when a pulse signal is outputted from the third selecting circuit 71-c at a timing T3, the shift register 75-b shifts the data to change the bit structure in a similar way to the above.

The AND circuit shown in FIG. 11 performs a control to output an enable signal to be used to read data stored in an address outputted from the adder 73. When values (numbers) outputted from the A column generating circuit 71 and the one row generating circuit 72 are predetermined values, respectively, the AND circuit 74 outputs an enable signal.

In concrete, when a value sent from the A column generating circuit 71 to the adder 73 corresponds to a multiple of "16" (decimal number) and any one of "0 to 368 (decimal numbers)", the first selecting circuit 71-a and the second selecting circuits 71-b output pulse signals to the AND circuit 71-d, and the AND circuit 71-d outputs a pulse signal to the AND circuit 74.

When a value sent from the one row generating circuit 72 to the adder 73 corresponds to any one of "0 to 15 (decimal numbers)", the fourth selecting circuit 72-a outputs a pulse signal to the AND circuit

74.

The AND circuit 74 outputs an enable signal to the first RAM 51 when receiving pulse signals from the AND circuit 71-d and the fourth selecting circuit 72-a.

For example, "255" outputted from the adder 73 to the first RAM 51 at a timing t26 in the foregoing Table 1 is used as an effective read address by that an enable signal is outputted from the AND circuit 74 to the first RAM 51 on the basis of pulse signals outputted from the AND circuit 71-d and the fourth selecting circuit 72-a, whereby the data stored at an address "255" is read out.

The A column generating circuit 71 and the one row generating circuit 72 shown in FIG. 10 are reset. However, in the structure shown in FIG. 11, the A column generating circuit 71 and the one row generating circuit 72 are not reset every cycle. Namely, the bit structure of the shift register 75-b becomes all "1" when a predetermined time is elapsed.

The de-interleaving unit (de-interleaving apparatus) 50-d shown in FIG. 5 de-interleaves received data.

In concrete, the de-interleaving unit 50-d arranges received data having been interleaved in a matrix, randomly rearranges at least either columns or rows of the data, and outputs the data in time

series, thereby outputting the received data in the order before the received data was interleaved.

In the case of the 384 of data (000-383) (refer to FIG. 9) interleaved by an interleaving unit 50-j in an another apparatus and sent from the another apparatus, the received data (000-383) is rearranged in the order before the received data was interleaved.

FIG. 13 is a block diagram showing the de-interleaving apparatus 50-d according to the first embodiment of this invention. As shown in FIG. 13, the de-interleaving apparatus 50-d comprises an interleaving RAM 53 and a control processing unit 54.

The interleaving RAM (second storing unit) 53 (hereinafter referred as "second RAM 53") stores received data.

The control processing unit (second control unit) 54 (hereinafter referred as "second control processing unit 54") controls the second RAM 53 so that the received data is outputted from the second RAM 53 in a state before the received data was interleaved by arranging the received data in a matrix and randomly rearranging columns and rows thereof.

To this end, the second control processing unit 54 comprises a write processing unit 60-1 (hereinafter referred as "second write processing

unit 60-1”) and a read processing unit (hereinafter referred as “second read processing unit 70-1”).

The write processing unit (second write processing unit) 60-1 generates an address used to write the received data in the second RAM 53 in a state before the received data was interleaved by arranging the received data in a matrix and randomly rearranging columns and rows thereof, thereby writing the received data.

For example, the write processing unit 60-1 performs a data writing control so that received data having been interleaved (refer to FIG. 9) is stored in the second RAM 53 in a state of the matrix shown in FIG. 6 by rearranging columns and rows thereof.

To this end, the second write processing unit 60-1 comprises, as shown in FIG. 13, an A column generating circuit 71, a one row generating circuit 72 and an adder 73.

The second write processing unit 60-1 comprising the A column generating circuit 71, the one row generating circuit and the adder 73 may, as shown in FIG. 11, also comprises an EX-OR 75-a, a shift register 75-b, a setting control unit 75-c, a first selecting circuit 71-a, a second selecting circuit 71-b, a third selecting circuit 71-c, an AND circuit 71-d, a fourth selecting circuit 72-a and a

switch (SW) 72-b, similarly to the above read processing unit 70. In the de-interleaving unit 50-d so structured, a number outputted from the adder 73 shown in FIG. 13 is used as a write address, as shown in FIG. 13.

The second read processing unit 70-1 shown in FIG. 13 reads data from the second RAM 53, outputs an address and an enable signal (not shown), and comprises a counter 61, as shown in FIG. 13.

Data read out from the second RAM 53 on the basis of a count value "0-383" which is sent from the counter 61 in the second read processing unit 70-1 is read out in numerical order as "000", "001", "002", "003", …, "150", …, 250", …, "382" and "383".

Since the MS 50 comprises the interleaving unit 50-j and the de-interleaving unit 50-d, the MS 50 has a function as an interleaving/de-interleaving apparatus which transmits/receives interleaved data to/from an opposite interleaving/de-interleaving apparatus.

The BS performing CDMA communication with the MS 50 transmits/receives data to/from the MS 50.

Now, the following description will be made by way of an example where interleaved data spread using the same spreading code is transmitted between the MS 50 and the BS in CDMA communication, and received data de-spread using the same de-spreading

code is de-interleaved.

The BS 100 comprises, as shown in FIG. 5, a receiver 50-a, a de-spreader 50-b, a data extracting unit 50-c, a de-interleaving unit (de-interleaving apparatus) 50-d, an error correction decoding unit 50-e, an error detecting unit 50-f, a CPU 50-g, an error detection encoding unit 50-h, an error correction encoding unit 50-i, an interleaving unit (interleaving apparatus) 50-j, a signal assembling unit 50-k, a spreader 50-l, a transmitter 50-m, a duplexer 50-n and an antenna 50-p, similarly to the foregoing MS 50.

Meanwhile, when CDMA communication uses a plurality of spreading codes, the BS 100 may be provided with the de-spreader 50-b and the spreader 50-l for each spreading code. Additionally, in order to process received data and data to be transmitted for each spreading code, the BS 100 may be provided with the data extracting unit 50-c, the de-interleaving unit 50-d, the error correction decoding unit 50-e, the error detecting unit 50-f, the error detection encoding unit 50-h, the error correction encoding unit 50-j, the interleaving unit 50-h and the signal assembling unit 50-k.

According to the MS 50 and the BS 100 each with the above structure according to the first embodiment, when the MS 50 transmits data to the BS 100, the MS

50 randomly rearranges columns and rows of data to which an error correcting code is added in the error correction encoding unit 50-i by the interleaving unit 50-j, and outputs the data in a state as shown in FIG. 9 to the signal assembling unit 50-k.

The interleaved data is assembled into a predetermined transmit data length by the signal assembling unit 50-k, then spread using a predetermined spreading code by the spreader 50-l. The spread interleaved data (digital signal) is converted or the like into an RF signal by the transmitter 50-m, then transmitted to the outside via the duplexer 50-n and the antenna 50-p.

On the other hand, when the BS 100 receives the RF signal transmitted from the MS 50 via the antenna 50-p and the duplexer 50-n, the receiver 50-a converts or the like the RF signal into a digital signal, and the de-spreader 50-b de-spreads the signal using a predetermined de-spreading code. After that, the data extracting unit 50-c extracts data having been interleaved by the interleaving unit 50-j in the MS 50, and the de-interleaving unit 50-d randomly rearranges columns and rows of the interleaved data to arrange the data in the order of before the interleaved data was interleaved, and sends the data to the error correction decoding unit 50-e.

The error correction decoding unit 50-e corrects a correctable error using an error correction code, and notifies of information on the error detected by the error detecting unit 50-f the CPU 50-g.

A processing on data to be transmitted from the BS 100 to the MS 50 is similar to the above, detailed description of which is omitted here.

According to the MS 50 and the BS 100 according to the first embodiment of this invention, even if data transmitted, for example, from the MS 50 to the BS 100 is affected by fading during transmission so that an error generates, the MS 50 on the transmitting side rearranges the data using relatively easy interleaving in a simple structure when transmitting the data so that distribution of the data is not biased, and transmits the data, and the BS 100 on the receiving side makes distribution of the error data be without bias using relatively easy de-interleaving in a simple structure when receiving the interleaved data, thereby preventing degradation of the transmission quality.

(b1-1) Description of a First Modification of the First Embodiment

Next, a first modification of the first embodiment will be described with reference to FIG. 5. An MS 50-1 and a BS 100-1 according to the first

modification of the first embodiment has similar functions to the MS 50 and the BS 100 according to the first embodiment. In contrast to the de-interleaving unit 50-d according to the first embodiment which randomly generates an address when received data is written in the second RAM 53, a de-interleaving unit according to the first modification of the first embodiment randomly generates an address used to read the data.

In the description of the first modification of the first embodiment, like reference characters designate like or corresponding parts in the first embodiment.

FIG. 14 is a diagram showing a structure of a de-interleaving unit 50-d1 according to the first modification of the first embodiment of this invention. As shown in FIG. 14, the de-interleaving unit 50-d1 comprises a second RAM 53-1 and a control processing unit 54-1.

The second RAM 53-1 stores received data, similarly to the second RAM 53.

The control processing unit (second control unit) 54-1 performs a control on the second RAM 53-1 so that received data is outputted from the second RAM 53-1 in a state before the received data was interleaved by arranging the received data in a matrix and randomly rearranging columns and rows

thereof, in a similar way to the second control processing unit 54 according to the first embodiment.

To this end, the control processing unit 54-1 comprises, as shown in FIG. 14, a write processing unit 60-2 (hereinafter referred as "third write processing unit 60-2") and a read processing unit 70-2 (hereinafter referred as "third read processing unit 70-2").

The third write processing unit 60-2 has a similar function to the first write processing unit 60 according to the first embodiment, which performs a control to write data in the second RAM 53-1, and outputs an address and an enable signal (not shown). The third write processing unit 60-2 comprises a counter 61.

On the other hand, the third read processing unit (second read processing unit) 70-2 generates a read address used to read the received data from the second RAM 53-1 in a state before the received data was interleaved by arranging the received data written in the second RAM 53-1 in a matrix and randomly rearranging columns and rows thereof.

To this end, the third read processing unit 70-2 comprises an A column generating circuit 71-1, a one row generating circuit 72-1 and an adder 73.

Although the A column generating circuit 71-1 has a similar function to the A column generating

circuit 71 according to the first embodiment, the A column generating circuit 71-1 generates numbers different from those generated by the A column generating circuit 71.

In concrete, as contrasted with the A column generating circuit 71 generating 24 numbers, the A column generating circuit 71-1 generates 16 numbers. However, the numbers generated by the A column generating circuit 71 and the numbers generated by the A column generated circuit 71-1 are different from each other. The numbers generated by the A column generating circuit 71-1 are "000", "144", "120", "216", "096", "312", "192", "360", "072", "048", "288", "240", "168", "264", "336" and "024", when described in the order generated.

Although the one row generating circuit 72-1 has a similar function to the one row generating circuit 72 according to the first embodiment, numbers generated by the one row generating circuit 72-1 are different from those generated by the one row generating circuit 72.

In concrete, the one row generating circuit 72 generates 16 numbers, whereas the one row generating circuit 72-1 generates 24 numbers. Furthermore, numbers generated by the one row generating circuit 72 and the one row generating circuit 72-1 are different from each other. The

numbers generated by the one row generating circuit 72-1 are "000", "008", "007", "013", "006", "019", "012", "021", "005", "003", "018", "015", "011", "016", "020", "010", "004", "009", "002", "022", "017", "010", "014" and "023", when described in the order generated.

FIG. 15 is a diagram showing values outputted from the A column generating circuit 71-1, the one row generating circuit 72-1 and the adder 73. As shown in FIG. 15, a value obtained by adding values outputted from the A column generating circuit 71-1 and the one row generating circuit 72-1 is outputted from the adder 73, and used as a read address.

When 16 numbers are completed to be outputted from the A column generating circuit 71-1, the one row generating circuit 72-1 outputs a different number, as shown in FIG. 15. Broken line α shown in FIG. 15 shows a change of the data outputted from the one row generating circuit 72-1.

The A column generating circuit 71-1 and the one row generating circuit 72-1 according to the first modification may be configured in a similar way to the A column generating circuit 71 and the one row generating circuit 72 shown in FIG. 11, respectively. However, the first selecting circuit 71-a selects a multiple of "24", while the fourth selecting circuit 72-a outputs a pulse signal when the value falls

within "0-23".

According to the MS 50-1 and the BS 100-1 with the foregoing structures, data interleaved in the MS 50-1 is rearranged in the order before the interleaved data was interleaved by the de-interleaving unit 50-d1 in the BS 100-1.

According to the MS 50-1 and the BS 100-1 according to the first embodiment of this invention, even if data transmitted from the MS 50-1 to the BS 100-1 is affected by fading that errors are generated in the transmitted data, for example, the MS 50-1 on the transmitting side having a simple structure rearranges the data using relatively easy interleaving so that distribution of the errors is not biased, while the BS 100-1 on the receiving side having a simple structure makes the distribution of the errors of the data be not biased when receiving the interleaved data, thereby preventing degradation of the transmission quality.

In the MS 50-1 and the BS 100-1, it is alternatively possible to replace the interleaving unit 50-j randomly generating a read address to be used to read data from the first RAM 51 in interleaving with an interleaving unit 50-j1 as shown in FIG. 16 randomly generating a write address used to write data in the first RAM 51-1.

In such case, the interleaved data is de-

interleaved using the de-interleaving unit 50-d according to the first embodiment.

The interleaving unit 15-1 comprises, as shown in FIG. 16, a first RAM 51-1 and a control processing unit 52-1.

The first RAM 51-1 stores data to be transmitted, similarly to the first RAM 51.

The control processing unit 52-1 performs a control on the first RAM 51-1 so that data to be transmitted is outputted from the first RAM 51-1 with the data to be transmitted arranged in a matrix and columns and rows thereof randomly rearranged, in a similar manner to the first control processing unit 52 according to the first embodiment.

To this end, the control processing unit 52-1 comprises, as shown in FIG. 16, a write processing unit 60-3 (hereinafter referred as "fourth write processing unit 60-3") and a read processing unit 70-3 (hereinafter referred as "fourth read processing unit 70-3).

The fourth read processing unit 70-3 functions in a similar manner to the second read processing unit 60-2 according to the first embodiment. The fourth read processing unit 70-3 performs a control to read data from the first RAM 51-1, and comprises a counter 61.

The fourth write processing unit (first write

control unit) 60-3 performs a control on the first RAM 51-1 so that data to be transmitted is outputted from the first RAM 51-1 with the data to be transmitted arranged in a matrix and columns and rows thereof randomly rearranged.

To this end, the fourth write processing unit 60-3 comprises an A column generating circuit 71-1, a one row generating circuit 72-1 and an adder 73.

The A column generating circuit 71-1 and the one row generating circuit 72-1 of the interleaving unit 50-j1 may be configured in a similar way to the A column generating circuit 71 and the one row generating circuit 72 shown in FIG. 11, respectively. However, the first selecting circuit 71-a selects a multiple of "24", and the fourth selecting circuit 72-a outputs a pulse signal when the value falls within "0-23".

The de-interleaving unit 50-d randomly rearranges columns and rows of data interleaved by the interleaving unit 50-j1, and reads the data in the order before the interleaved data was interleaved. A combination of the interleaving unit 50-j1 and the de-interleaving unit 50-d can readily prevent degradation of the transmission quality as well even if burst errors generate during transmission.

(b1-2) Description of a Second Modification of the First Embodiment

Next, description will be made of a second modification of the first embodiment with reference to FIG. 5. An MS 50-2 and a BS 100-2 according to the second modification of the first embodiment have similar functions to the MS 50 and the BS 100 according to the first embodiment, respectively. Differently from the MS 50 and the BS 100 according to the first embodiment, the structure of the interleaving unit 50-j according to the first embodiment shown in FIG. 10 and the structure of the de-interleaving unit 50-d according to the first embodiment shown in FIG. 13 are exchanged to each other to form an interleaving unit 50-j2 and a de-interleaving unit 50-d2.

In the description of the second modification of the first embodiment, like reference characters designate like or corresponding parts in the first embodiment.

The de-interleaving unit 50-d2 is configured in a similar manner to the interleaving unit 50-j, as shown in FIG. 10. The first RAM 51 shown in FIG. 10 stores input data sent from the data extracting unit 50-c, and outputs the data held therein to the error correction decoding unit 50-e under a control of the first read processing unit 70.

The interleaving unit 50-j2 is configured in a similar manner to the de-interleaving unit 50-d,

as shown in FIG. 13. The second RAM 53 shown in FIG. 13 stores input data sent from the error correction encoding unit 50-i under a control of the second write processing unit 60-1, and outputs the data held therein to the signal assembling unit 50-k under a control of the second read processing unit 70-1.

In the MS 50-2 and the BS 100-2 with the foregoing structures, even if data transmitted from the MS 50-2 to the BS 100-2 is affected by fading that errors are generated in the transmitted data, the MS 50-2 on the transmitting side randomly rearranges columns and rows of the data to be transmitted when transmitting, and the BS 100-2 on the receiving side rearranges the data in the order before the interleaved data was interleaved when receiving the interleaved data, in a similar way to the MS 50 and the BS 100 according to the first embodiment.

Accordingly, even if burst errors generate in 384 of data randomly rearranged on the transmitting side during transmission, the receiving side reforms the data into a readily correctable form to randomly distribute the errors, thereby readily correcting the errors, which prevents degradation of the transmission quality.

Incidentally, the above is the same even when the structures of the de-interleaving unit 50-d1 and the interleaving unit 50-j according to the first

modification of the first embodiment are exchanged, or structures of the interleaving unit 50-j1 and the de-interleaving unit 50-d are exchanged.

(b2) Description of a Second Embodiment

Next, description will be made of a second embodiment with reference to FIG. 5. An MS 50-3 and a BS 100-3 shown in FIG. 5 according to the second embodiment have similar functions to the MS 50 and the BS 100 according to the first embodiment, respectively. However, the BS 50-3 and the BS 100-3 are different from those according to the first embodiment in a point that each of the A column generating circuit 71 and the one row generating circuit 72 in the de-interleaving unit 50-d and the interleaving unit 50-j according to the first embodiment is configured with a ROM and a counter.

In the description of the second embodiment, like reference characters designate like or corresponding parts in the above first embodiment.

FIG. 17 is a block diagram showing a de-interleaving unit according to the second embodiment. As shown in FIG. 17, a de-interleaving unit 50-d3 comprises an A column generating circuit 71-2 and a one row generating circuit 72-2 along with a second RAM 53, an adder 73 and a counter 61, similar to those of the de-interleaving unit 50-d according to the first embodiment.

The A column generating circuit 71-2 comprises a similar function to the A column generating circuit 71 according to the first embodiment, but has a ROM (Read Only Memory) 71-2a and a counter 71-2b, as shown in FIG. 17. The ROM (memory) 71-2a holds 24 numbers (refer to FIG. 8) in the A column in predetermined addresses, respectively. Table 3 below shows an example of data held in the ROM 71-2a.

[table 3]

Example of held data

Address	0	1	2	3	4	5	6	7	…	20	21	22	23
Data	000	240	288	144	256	128	064	032	…	224	112	304	368

As shown in Table 3 above, the ROM 71-2a holds 24 numbers in column A shown in FIG. 8 in the descending order. For example, a number "256" is held in an address "4". When the ROM 71-2a receives a count value (address in Table 3 above) outputted from the counter 71-2b, the ROM 71-2a reads data held in that address, and outputs the data to the adder 73.

The counter 71-2b is a free-running counter, which counts from "0" to "23", outputs a count value as a read address for the ROM 71-2a, and again counts from "0" when the count value reaches a maximum count value "23". The counter 71-2b sends a carry pulse to the counter 72-2b (to be described later) when a

count cycle takes a round.

On the other hand, the one row generating circuit 72-2 has a similar function to the one row generating circuit 72 according to the first embodiment, but comprises a ROM 72-2a and a counter 72-2b, as shown in FIG. 17. The ROM (memory) 72-2a holds 16 numbers (refer to FIG. 8) in one row at predetermined addresses, respectively. Table 4 below shows an example of data held in the ROM 72-2a.

[table 4]

Example of held data

Address	0	1	2	3	4	5	6	7	…	12	13	14	15
data	000	015	009	008	004	002	001	012	…	010	005	014	007

As shown in Table 4 above, the ROM 72-2a holds 16 number in one row shown in FIG. 8 in order, from left to right. For example, a number "008" is held in an address "3". When the ROM 72-2a receives a count value (address in Table 4 above) outputted from the counter 72-2b, the ROM 72-2a reads data held in that address and outputs the data to the adder 73.

The counter 72-2b counts from "0" to "15", outputting a count value as a read address for the ROM 72-2a and again counting from "0" when the count value reaches a maximum count value "15". Incidentally, the counter 72-2b counts up by receiving a carry pulse from the counter 71-2b in the A column generating circuit 71-2.

Write addresses outputted from the adder 73 shown in FIG. 13 are the same as those in the example shown in Table 1.

FIG. 18 is a block diagram showing an interleaving unit according to the second embodiment. As shown in FIG. 18, an interleaving unit 50-j3 comprises an A column generating circuit 71-2 and a one row generating circuit 72-2 along with a first RAM 51, an adder 73 and a counter 61 similar to those of the interleaving unit 50-j according to the first embodiment.

According to the MS 50-3 and the BS 100-3 with the above structures according to the second embodiment, when the MS 50-3 transmits data to the BS 100-3, the interleaving unit 50-j3 of the MS 50 randomly shuffles columns and rows of the data to be transmitted, and sends the interleaved data in the order as shown in FIG. 9 to the signal assembling unit 50-k, in a similar manner to the MS 50 and the BS 100 according to the first embodiment.

In interleaving, the interleaving unit 50-j3 reads data stored in the first RAM 51 using a value obtained by adding data (refer to foregoing Tables 3 and 4) sent from ROM 71-2a and the ROM 72-2a by the adder 73 as a read address to randomly read 384 of data (000-383).

After that, the interleaved data is sent to

the BS 100-3 via the spreader 50-1, etc.

The BS 100-3 receives the data sent from the MS 50-1 via the de-spreader 50-b, etc., de-interleaves the data by the de-interleaving unit 50-d3, and sends the data in the order before the interleaved data was interleaved to the error correction decoding unit 50-e.

In de-interleaving, the de-interleaving unit 50-d3 reads data stored in the second RAM 53 using a value obtained by adding data (refer to foregoing Tables 3 and 4) sent from the ROM 71-2a and the ROM 72-2a as a write address to randomly write 384 of data in the second RAM 53. After writing the data in the second RAM 53, the de-interleaving unit 50-d3 performs a control to read the 384 of data in order, beginning with a count value "0" of the counter 61.

According to the MS 50-3 and the BS 100-3 with the above structures, it is possible in random generation to readily set an order or the like in which 26 numbers in column A and 16 numbers in one row are to be generated, which becomes a reference for address generation, using the ROMs 71-2a and 72-2a, and certainly rearrange 384 of data (000-383), in addition to the effects described in the first embodiment, thereby preventing degradation of the transmission quality.

(b2-1) Description of a Modification of the Second

Embodiment

Next, description will be made of a modification of the second embodiment with reference to FIG. 5. An MS 50-4 and a BS 100-4 according to the modification of the second embodiment shown in FIG. 5 have similar functions to the MS 50-3 and the BS 100-3 according to the second embodiment, respectively, but are different from those according to the second embodiment in a point that a ROM is used to randomly generate an address when data is interleaved or de-interleaved, unlike the de-interleaving unit 50-d3 and the interleaving unit 50-j3 according to the second embodiment.

In the description of the modification of the second embodiment, like reference characters designate like or corresponding parts in the second embodiment.

Each of the MS 50-4 and the BS 100-4 comprises a de-interleaving apparatus 50-d1 according to the first modification of the first embodiment in lieu of the de-interleaving unit 50-d3 according to the second embodiment.

In the MS 50-4 and the BS 100-4 with the above structures, it is possible to randomly rearrange columns and rows of data to be transmitted to form interleaved data as shown in FIG. 9 on the transmitting side, and randomly rearrange columns

and rows of the interleaved data and send the data in the order before the interleaved data was interleaved to the error correction encoding unit 50-e on the receiving side, in a similar manner to the first and second embodiments. Even if burst errors generate during transmission, it is thereby possible to prevent degradation of the transmission quality by distributing errors such that the errors can be readily corrected. In addition, use of the ROMs 71-2a and 72-2a in random generation facilitates easy setting of an order or the like in which 24 numbers in column A and 16 numbers in one row are to be generated, which becomes a reference for address generation, thereby certainly rearranging 384 of data (000-383), which leads to prevention against degradation of the transmission quality.

Each of the MS 50-4 and the BS 100-4 may be provided with the interleaving apparatus 50-j1 according to the first modification of the first embodiment in lieu of the interleaving unit 50-j3 according to the second embodiment. In such case, it is possible to prevent degradation of the transmission quality, as well. In addition, the random generation on the receiving side can be readily realized using the ROMs 71-2a and 72-2a.

(b3) Others

The above description has been made by way of

CDMA communication. However, the present invention can be carried out in a similar manner as far as other radio communication has a function of correcting an error by using an error correcting code.

In the above description, the interleaving unit 50-j interleaves data to which an error correcting code is added in the error correction encoding unit 50-i. However, the error correction encoding unit 50-i may have a function of interleaving when a turbo code is used as the error correcting code. Incidentally, a turbo code is a code in combination of a convolution code, a BCH code, a Reed-Solomon code and interleaving.

For example, FIG. 19 is a diagram showing an error correction encoding unit 50-i1 having an interleaving function. The error correction encoding unit 50-i1 shown in FIG. 19 comprises an interleaving unit 50-j and encoding apparatus 50-ia.

The encoding apparatus 50-ia (designated as "ENC" in the drawing) performs convolution or the like.

When data u is inputted to the error correction encoding unit 50-i1 shown in FIG. 19, the data u is formed into three signals X_a, X_b, and X_c through the encoding apparatus 50-ia, the interleaving unit 50-j, etc. The data X_a, X_b, and X_c are sent to the

interleaving unit 50-j, interleaved, respectively, and transmitted to the outside via the spreader 50-1, etc.

On the other hand, data y_a, y_b, and y_c on the receiving side (assuming that X_a, X_b, and X_c are modified into y_a, y_b, and y_c, respectively, by an effect of fading during transmission) is sent to the error correction decoding unit 50-e1 shown in FIG. 20.

The error correction decoding unit 50-e1 comprises, as shown in FIG. 20, decoding apparatus 50-ea, an interleaving unit 50-j and a de-interleaving unit 50-d.

The decoding apparatus 50-ea performs convolution decoding and the like.

In the error correction decoding unit 50-e1, a degree of correlation among the data y_a, y_b, and y_c is decreased, and the data whose error rate is decreased is sent to the error detecting unit 50-f. In concrete, the interleaving unit 50-j interleaves data y_a' obtained by decoding the data y_a and y_b. Data y_a'' obtained by decoding the interleaved data and the data y_c is further de-interleaved.

The error correction decoding unit 50-e1 performs a processing similar to decoding or the like with the data de-interleaved by the de-interleaving

unit 50-d and the data y_b, and outputs decoded data u′ whose correlation has been decreased.

As above, with a turbo code, it is possible to improve a weight distribution of the turbo code.

Alternatively, it is possible to separately rearrange the columns and rows shown in FIGS. 6 through 8.

FIG. 21 is a block diagram showing an interleaving unit 50-j5. The interleaving unit 50-j5 comprises interleaving RAMS 56A through 56C, counters 61A through 61C, adders 73 through 75, row generating circuits 71A, 72B and 72C, and column generating circuits 72A, 71B and 71C.

Each of the interleaving RAMs (first storing unit) 56A through 56C is similar to the first RAM 51, which stores data to be transmitted.

Each of the row generating circuit 71A and the column generating circuits 71B and 71C has a similar function to the A column generating circuit, which outputs a different number at each timing to the adder. The row generating unit 71A outputs 16 numbers in one row shown in FIG. 7. The column generating circuit 71B generates numbers (000-015) in order, beginning with "000". The column generating circuit 71C generates "000" and multiples of 16 among numbers (000-368) in order, beginning with "000" up to "368".

Each of the column generating circuit 72A and

the row generating circuits 72B and 72C has a similar function to the one row generating circuit 72. The column generating circuit 72A generates numbers (000-015) in order, beginning with "000". The row generating circuit 72B generates 24 numbers in column A shown in FIG. 8 in the descending order. The row generating circuit 72C generates numbers (000-015) in order, beginning with "000".

Each of the column generating circuit 72A and the row generating circuits 72B and 72C varies a number to be outputted to the adder 73 with reception of a carry pulse from the corresponding row generating circuit 71A, the column generating circuit 71B or 71C as an opportunity.

The interleaving apparatus 50-j5 shown in FIG. 21 rearranges the data (000-383) as shown in FIGS. 6 through 8, so that the data is arranged in the order shown in FIG. 9.

FIGS. 25 through 32 are diagrams for illustrating interleaving (24[4[2×2]×6[3×2]]×16[4[[2×2]×4[2×2]]). Hereinafter, description will be made of interleaving (24[4[2×2]×6[3×2]]×16[4[[2×2]×4[2×2]]). 384 of data are arranged in a matrix of 24 rows by 16 columns as shown in FIG. 25.

Interleaving rearranges 16 columns in the order shown in FIG. 25 (1-16 shown in FIG. 25). FIG.

26 is a diagram showing a state where the 384 of data are arranged after the columns thereof shown in FIG. 25 are rearranged.

16 columns of the 384 of data are then divided into 4 groups, and the groups each consisting of 4 columns are rearranged in the order numbered (1-4 in FIG. 26). FIG. 27 is a diagram showing a state where the 384 of data whose columns shown in FIG. 26 have been rearranged.

The 384 of data whose 16 columns have been divided into 4 groups are rearranged in each group consisting of 4 columns in the order numbered (1-4 shown in FIG. 27). FIG. 28 is a diagram showing a state in which the 384 of data whose columns have been rearranged are arranged.

Next, 24 rows of the 384 of data are rearranged in the order numbered as shown in FIG. 28 (1-24 shown in FIG. 28). FIG. 29 is a diagram showing a state where the 384 of data are arranged after the rows thereof have been rearranged.

Further, the 24 rows of the 384 data are divided into 6 groups, and the rows in each group are rearranged in the order numbered (1-6 shown in FIG. 29). FIG. 30 is a diagram showing a state where the 384 of data whose rows shown in FIG. 29 have been rearranged are arranged.

The 384 of data are then divided in to 6 groups

as shown in FIG. 30, and rearranged in each group consisting of 4 rows in the order numbered (1-4 shown in FIG. 30). FIG. 31 is a diagram showing a state where the 384 of data whose rows shown in FIG. 30 have been rearranged are arranged.

The 384 of data are read out in the direction of column as "000", "192", "096", "288", "032", "224" "128" and so on. When 24 of data in one column are completed, the data are again read out in the direction of row, beginning with the head of the column on the right.

For example, when reading of the last "368" in the column including "000" shown in FIG. 31 is completed, "008" at the head of the column on the right is next read out.

FIG. 32 is a diagram showing a state where interleaved 368 of data are arranged. The interleaved 368 of data shown in FIG. 32 are arranged, beginning with "000", in a direction from left to right, the data "368" shown at the right end is followed by "008", "376" is followed by "004", and so on.

The above interleaving (24[4[2×2]×6[3×2]] ×16[4[[2×2]×4[2×2]]) can be readily carried out using the above A column generating circuit 71 or the like, and the above one row generating circuit 72 or the like.

For example, the A column generating circuit 71 or the like is so configured as to generate 24 numbers ("000", "192", "096", "288", "032", "224", "128", "320", "064", "256", "160", "352", "016", "208", "112", "304", "048", "240", "144", "336", "080", "272", "176" and "386" in the order generated) in column A′ shown in FIG. 31.

The one row generating circuit 72 or the like is so configured as to generate 16 numbers ("000", "008", "004", "012", "002", "010", "006", "014", "001", "009", "005", "013", "003", "011", "007" and "015" in the order generated) in row 1′ shown in FIG. 31.

Meanwhile, the present invention can perform not only the above interleaving (24[4[2×2]×6[3×2]]×16[4[[2×2]×4[2×2]]]), but also (20[4[2×2]×5[3×2]]×16[4[[2×2]×4[2×2]]]) or the like.

The above description has been made by way of example where columns and rows are randomly shuffled. However, it is alternatively possible to randomly shuffle either columns or rows to rearrange data.

Further, the above description has been made by way of example where the ROM 71-2a or the like is used as a memory. However, it is alternatively possible to use another storage element as the memory.

Note that the present invention is not limited

to the above examples, but may be modified in various ways without departing from the scope of the invention.